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What is claimed is:

1. A method of performing a design of an integrated circuit comprising:

defining a physical design of the circuit while tracking an error in prediction of a timing value associated with one or more nets in the circuit; and

determining a physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold.

2. The method of claim 1, wherein the defining the physical design further comprises performing a soft placement of the design.

3. The method of claim 2, wherein the performing the soft placement of the design further comprises performing one or more of the following: placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design.

4. The method of claim 2, wherein the performing the soft placement of the design further comprises simultaneously performing one or more of the following in parallel: placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design.

5. The method of claim 1, wherein the determining the physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold further comprises:

localizing placement of cells and wires in the physical design;

creating a profile of the wire lengths from the physical design;

calculating an error in a prediction of a timing value from the profile of the wire lengths; and

comparing the error in the prediction of the timing value with the predetermined threshold to determine if the error satisfies the predetermined threshold.

6. The method of claim 1, wherein the determining the physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold further comprises:

(a) quadrisectioning the physical design into bins;

(b) localizing placement of cells and wires of the physical design into the bins;

(c) creating a profile of the wire lengths in each of the bins;

(d) calculating a plurality of errors in a prediction of timing values from the profile of the wire lengths for each bin respectively;

(e) comparing each of the plurality of errors in the prediction of the timing values with the predetermined threshold to determine if the error satisfies the predetermined threshold; and either:

further quadrisectioning the physical design and repeating (b through e); or

generating an interrupt if all of the plurality of errors in the prediction of the timing values for each of the bins satisfy the predetermined threshold.

7. The method of claim 6, wherein the creating a profile of the wire lengths in each of the bins further comprises plotting wire lengths versus instances of nets in each of the bins.

8. The method of claim 1, further comprising performing interactive optimization of the physical design after the error in prediction of the timing value satisfies the predetermined threshold.

9. The method of claim 1, further comprising analyzing one or more of the following characteristics of the physical design after the error in prediction of the timing value satisfies the predetermined threshold: congestion, timing, power, and signal integrity.

10. The method of claim 9, further comprising generating a report indicative of the congestion, timing, power, signal integrity of the physical design.

11. The method of claim 1, further comprising:

performing a second physical design of the circuit derived from the physical design of the circuit performed while tracking the error in prediction of the timing value associated with one or more nets in the circuit; and

generating a GDS file from the second physical design of the circuit.

12. The method of claim 11, wherein the performing the second physical design of the circuit further comprises simultaneously performing one or more of the following in parallel: placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design.

13. A computer-readable medium including computer code configured to perform the design of an integrated circuit, the computer code configured to effectuate the following:

defining a physical design of the circuit while tracking an error in prediction of a timing value associated with one or more nets in the circuit; and

determining a physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold.

14. The computer code of claim 13, wherein the defining the physical design further comprises performing a soft placement of the design.

15. The computer code of claim 14, wherein the performing the soft placement of the design further comprises performing one or more of the following: placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design.

16. The computer code of claim 14, wherein the performing the soft placement of the design further comprises simultaneously performing one or more of the following in parallel: placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design.

17. The computer code of claim 13, wherein the determining the physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold further comprises:

localizing placement of cells and wires in the physical design;

creating a profile of the wire lengths from the physical design;

calculating an error in a prediction of timing value from the profile of the wire lengths; and

comparing the error in the prediction of the timing value with the predetermined threshold to determine if the error satisfies the predetermined threshold.

18. The computer code of claim 13, wherein the determining the physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold further comprises:

(a) quadrisectioning the physical design into bins;

(b) localizing placement of cells and wires of the physical design into the bins;

(c) creating a profile of the wire lengths in each of the bins;

(d) calculating a plurality of errors in a prediction of timing values from the profile of the wire lengths for each bin respectively;

(e) comparing each of the plurality of errors in the prediction of the timing values with the predetermined threshold to determine if the error satisfies the predetermined threshold; and either:

further quadrisectioning the physical design and repeating (b through e);. or

generating an interrupt if all of the plurality of errors in the prediction of the timing values for each of the bins satisfy the predetermined threshold.

19. The computer code of claim 18, wherein the creating a profile of the wire lengths in each of the bins further comprises plotting wire lengths versus instances of nets in each of the bins.

20. The computer code of claim 13, further configured to effectuate performing interactive optimization of the physical design after the error in prediction of the timing value satisfies the predetermined threshold.

21. The computer code of claim 13, further configured to effectuate analyzing one or more of the following characteristics of the physical design after the error in prediction of the timing value satisfies the predetermined threshold: congestion, timing, power, and signal integrity.

22. The computer code of claim 21, further configured to effectuate generating a report indicative of the congestion, timing, power, signal integrity of the physical design.

23. The computer code of claim 13, wherein the computer code is further configured to effectuate:

performing a second physical design of the circuit derived from the physical design of the circuit performed while tracking the error in prediction of the timing value associated with one or more nets in the circuit; and

generating a GDS file from the second physical design of the circuit.

24. The computer code of claim 23, wherein the performing the second physical design of the circuit further comprises simultaneously performing one or more of the following in parallel: placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design.

25. A computer system configured to perform the design of an integrated circuit, the computer system comprising:

a physical design module configured to define a physical design of the circuit while tracking an error in prediction of a timing value associated with one or more nets in the circuit; and

a physical placement level module configured to determine a physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold.

26. The computer system of claim 25, wherein the physical design module is further configured to perform a soft placement of the design.

27. The computer system of claim 26, wherein the physical design module is further configured to perform one or more of the following: placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design.

28. The computer system of claim 26, wherein the physical design module is further configured to simultaneously performing one or more of the following in parallel: placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design.

29. The computer system of claim 25, wherein the physical placement level module is configured to determine the physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold by:

localizing placement of cells and wires in the physical design;

creating a profile of the wire lengths from the physical design;

calculating an error in a prediction of timing value from the profile of the wire lengths; and

comparing the error in the prediction of the timing value with the predetermined threshold to determine if the error satisfies the predetermined threshold.

30. The computer system of claim 25, wherein the physical placement level module is configured to determine the physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold by:

(a) quadrisectioning the physical design into bins;

(b) localizing placement of cells and wires of the physical design into the bins;

(c) creating a profile of the wire lengths in each of the bins;

(d) calculating a plurality of errors in a prediction of timing values from the profile of the wire lengths for each bin respectively;

(e) comparing each of the plurality of errors in the prediction of the timing values with the predetermined threshold to determine if the error satisfies the predetermined threshold; and either:

further quadrisectioning the physical design and repeating (b through e); or

generating an interrupt if all of the plurality of errors in the prediction of the timing values for each of the bins satisfy the predetermined threshold.

31. The computer system of claim 30, wherein the creating a profile of the wire lengths in each of the bins further comprises plotting wire lengths versus instances of nets in each of the bins.

32. The computer system of claim 25, further comprising a prototype optimization tool to optimize the physical design after the error in prediction of the timing value satisfies the predetermined threshold.

33. The computer system of claim 25, wherein the prototype optimization tool further comprises analyzing one or more of the following characteristics of the physical design after the error in prediction of the timing value satisfies the predetermined threshold: congestion, timing, power, and signal integrity.

34. The computer system of claim 33, further comprising a report generating tool configured to generate a report indicative of the congestion, timing, power, signal integrity of the physical design.

35. The computing system of claim 25, further comprising:

a second physical design tool configured to perform a second physical design of the circuit derived from the physical design of the circuit performed while tracking the error in prediction of the timing value associated with one or more nets in the circuit; and

a GDS tool configured to generate a GDS file from the second physical design of the circuit.

36. The computing system of claim 35, wherein the second physical design tool is configured to perform the second physical design of the circuit by simultaneously performing one or more of the following in parallel: placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design.

37. A method of designing an integrated circuit comprising:

performing estimates of physical area placement and timing analysis on a circuit design defined by a net list;

refining a physical placement of the circuit design based on the estimates of physical area placement and timing analysis; and

generating a prototype indicative of the refined physical placement of the circuit design.

38. The method of claim 37, wherein the performing estimates of physical area placement and timing analysis on the circuit design defined by the net list further comprise:

performing a soft placement of the circuit design into bins;

calculating errors in prediction of timing values of the circuit design in the bins;

comparing the errors of prediction of timing values for the bins to a predetermined threshold; and

repeating the performing the soft placement of the circuit design into smaller and smaller bins and calculating the error in prediction of the timing values from the soft placement of the circuit design until all the errors of prediction of the timing values satisfy the predetermined threshold.

39. The method of claim 38, wherein the refining the physical placement of the circuit design further comprises the quantizing the circuit design into the bins and performing placement of cells and wires of the circuit design into the bins with each repetition.

40. The method of claim 37, wherein the refining the physical placement of the circuit design further comprises the repeatedly quantizing the circuit design into smaller and smaller bins and performing placement of cells and wires of the circuit design into the bins with each repetition.

41. The method of claim 40, further comprises for each repetition:

(a) creating a profile of the wire lengths versus the instances of nets for each of the bins;

(b) comparing the errors of prediction of timing values for each of the bins to the predetermined threshold;

repeating steps (a) and (b) until the all of the errors of prediction for each of the bins satisfy the predetermined threshold; and

generating the prototype based on the placement of the circuit design after all of the errors of prediction for each of the bins satisfy the predetermined threshold.

42. The method of claim 38, wherein the performing the physical placement of the circuit design further comprises performing one or more of the following: placement of cells of the circuit design, logic optimization of the circuit design, routing of wires in the circuit design, timing and clock control for the circuit design and extraction of the circuit design.

43. The method of claim 37, further comprising performing interactive optimization to the prototype to generate a sign-off prototype.

44. The method of claim 37, further comprising analyzing one or more of the following characteristics of the circuit design defined by the prototype: congestion, timing, power, and signal integrity.

45. The method of claim 44, further comprising generating a report indicative of one or more of the following characteristics regarding the circuit design: congestion, timing, power, signal integrity of the circuit design defined by the prototype.

46. The method of claim 37, further comprising:

creating a physical design of the circuit design derived from the prototype; and

generating a GDS file after creating the physical design of the circuit.

47. The method of claim 46, wherein the creating the physical design of the circuit design further comprises simultaneously performing one or more of the following in parallel: placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design.

48. A computer-readable medium comprising computer code configured to perform the design of an integrated circuit, the computer code configured to effectuate the following:

performing estimates of physical area placement and timing analysis on a circuit design defined by a net list;

refining a physical placement of the circuit design based on the estimates of physical area placement and timing analysis; and

generating a prototype indicative of the refined physical placement of the circuit design.

49. The computer code of claim 48, wherein the performing estimates of physical area placement and timing analysis on the circuit design defined by the net list is further configured to effectuate:

performing a soft placement of the circuit design into bins;

calculating errors in prediction of timing values of the circuit design in the bins;

comparing the errors of prediction of timing values for the bins to a predetermined threshold; and

repeating the performing the soft placement of the circuit design and calculating the error in prediction of the timing values from the soft placement of the circuit design until all the errors of prediction of the timing values satisfy the predetermined threshold.

50. The computer code of claim 49, wherein the refining the physical placement of the circuit design further comprises the quantizing the circuit design into the bins and performing placement of cells and wires of the circuit design into the bins with each repetition.

51. The computer code of claim 48, wherein the refining the physical placement of the circuit design further comprises repeating the quantizing the circuit design into smaller and smaller bins and performing placement of cells and wires of the circuit design into the bins with each repetition.

52. The computer code of claim 51, further configured to effectuate for each repetition:

(a) creating a profile of the wire lengths versus the instances of nets for each of the bins;

(b) comparing the errors of prediction of timing values for each of the bins to the predetermined threshold;

repeating steps (a) and (b) until the all of the errors of prediction for each of the bins satisfy the predetermined threshold; and

generating the prototype based on the placement of the circuit design after all of the errors of prediction for each of the bins satisfy the predetermined threshold.

53. The computer code of claim 49, wherein the performing the physical placement of the circuit design further comprises performing one or more of the following: placement of cells of the circuit design, logic optimization of the circuit design, routing of wires in the circuit design, timing and clock control for the circuit design and extraction of the circuit design.

54. The computer code of claim 48, further configured to include an optimization tool that enables the optimization of the prototype to generate a sign-off prototype.

55. The computer code of claim 48, further configured to effectuate analyzing one or more of the following characteristics of the circuit design defined by the prototype: congestion, timing, power, and signal integrity.

56. The computer code of claim 55, further configured to effectuate generating a report indicative of one or more of the following characteristics regarding the circuit design: congestion, timing, power, signal integrity of the circuit design defined by the prototype.

57. The computer code of claim 56, further configured to effectuate:

creating a physical design of the circuit design derived from the prototype; and

generating a GDS file after creating the physical design of the circuit.

58. The computer code of claim 57, wherein the creating the physical design of the circuit design further comprises simultaneously performing one or more of the following in parallel: placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design.

59. A system configured to design an integrated circuit, the system comprising:

a computer system configured to:

perform estimates of physical area placement and timing analysis on a circuit design defined by a net list;

refine a physical placement of the circuit design based on the estimates of physical area placement and timing analysis; and

generate a prototype indicative of the refined physical placement of the circuit design.

60. The system of claim 59, wherein the performing estimates of physical area placement and timing analysis on the circuit design defined by the net list further comprise:

performing a soft placement of the circuit design into bins;

calculating errors in prediction of timing values of the circuit design in the bins;

comparing the errors of prediction of timing values for the bins to a predetermined threshold; and

repeating the performing the soft placement of the circuit design into smaller and smaller bins and calculating the error in prediction of the timing values from the soft placement of the circuit design until all the errors of prediction of the timing values satisfy the predetermined threshold.

61. The system of claim 60, wherein the refining the physical placement of the circuit design further comprises the quantizing the circuit design into the bins and performing placement of cells and wires of the circuit design into the bins with each repetition.

62. The system of claim 61, wherein the refining the physical placement of the circuit design further comprises the repeatedly quantizing the circuit design into smaller and smaller bins and performing placement of cells and wires of the circuit design into the bins with each repetition.

63. The system of claim 62, further comprises for each repetition:

(a) creating a profile of the wire lengths versus the instances of nets for each of the bins;

(b) comparing the errors of prediction of timing values for each of the bins to the predetermined threshold;

repeating steps (a) and (b) until the all of the errors of prediction for each of the bins satisfy the predetermined threshold; and

generating the prototype based on the placement of the circuit design after all of the errors of prediction for each of the bins satisfy the predetermined threshold.

64. The system of claim 60, wherein the performing the physical placement of the circuit design further comprises performing one or more of the following: placement of cells of the circuit design, logic optimization of the circuit design, routing of wires in the circuit design, timing and clock control for the circuit design and extraction of the circuit design.

65. The system of claim 59, wherein the computing system further comprises a prototype optimization tool to perform optimization on the prototype to generate a sign-off prototype.

66. The system of claim 59, further comprising an tool to analyze one or more of the following characteristics of the circuit design defined by the prototype: congestion, timing, power, and signal integrity.

67. The system of claim 66, further comprising a report tool configured to generate a report indicative of one or more of the following characteristics regarding the circuit design: congestion, timing, power, signal integrity of the circuit design defined by the prototype.

68. The system of claim 59, wherein the computing system is further configured to:

create a physical design of the circuit design derived from the prototype; and

generate a GDS file after creating the physical design of the circuit.

69. The system of claim 68, wherein the computing system is further configured to simultaneously performi one or more of the following in parallel when creating the physical design of the circuit: placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design.

70. A method for a first party to fabricate a semiconductor device, comprising:

receiving an sign-off prototype, the sign-off prototype generated by:

defining a physical design of a circuit while tracking an error in prediction of a timing value associated with one or more nets in the circuit;

determining a physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold; and

generating the sign-off prototype from the physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold; and after receiving the sign-off prototype, the first party performing:

generating a second physical design of the circuit from the sign-off prototype;

generating a GDS file from the second physical design;

having a mask set generated from the GDS file; and

having the semiconductor device fabricated using the mask set.

71. The method of claim 70, wherein generating the second physical design of the circuit further comprises performing one or more of the following: placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design.

72. The method of claim 71, wherein the performing the placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design occurs substantially in parallel using a physical design tool.

73. The method of claim 70, wherein the receiving the sign-off prototype further comprises receiving the sign-off prototype from a second party.

74. The method of claim 73, generating the second physical design of the circuit from the sign-off prototype further comprises having the second party to perform additional interactive optimization on the sign-off prototype after receiving the sign-off prototype so the second party can collaborate in resolving problems identified in the sign-off prototype.

75. The method of claim 70, wherein the determining the physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold further comprises:

(a) quadrisectioning the physical design into bins;

(b) localizing placement of cells and wires of the physical design into the bins;

(c) creating a profile of the wire lengths in each of the bins;

(d) calculating a plurality of errors in a prediction of timing values from the profile of the timing values for each bin respectively;

(e) comparing each of the plurality of errors in the prediction of the timing values with the predetermined threshold to determine if the timing value satisfies the predetermined threshold; and either:

further quadrisectioning the physical design and repeating (b through e); or

generating an interrupt if all of the plurality of errors in the prediction of the timing values for each of the bins satisfy the predetermined threshold.

76. A semiconductor device manufactured by a first party by:

receiving an sign-off prototype, the sign-off prototype generated by:

defining a physical design of a circuit while tracking an error in prediction of a timing value associated with one or more nets in the circuit;

determining a physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold; and

generating the sign-off prototype from the physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold; and after receiving the sign-off prototype: and

after receiving the sign-off prototype, the first party performing:

generating a second physical design of the circuit from the sign-off prototype;

generating a GDS file from the second physical design;

having a mask set generated from the GDS file; and

having the semiconductor device fabricated using the mask set.

77. The semiconductor device of claim 76, wherein generating the second physical design of the circuit further comprises performing one or more of the following: placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design.

78. The semiconductor device of claim 77, wherein the performing the placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design occurs substantially in parallel using a physical design tool.

79. The semiconductor device of claim 76, wherein the determining the physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold further comprises:

(a) quadrisectioning the physical design into bins;

(b) localizing placement of cells and wires of the physical design into the bins;

(c) creating a profile of the wire lengths in each of the bins;

(d) calculating a plurality of errors in a prediction of timing values from the profile of the wire lengths for each bin respectively;

(e) comparing each of the plurality of errors in the prediction of the timing values with the predetermined threshold to determine if the timing value satisfies the predetermined threshold; and either:

further quadrisectioning the physical design and repeating (b through e); or

generating an interrupt if all of the plurality of errors in the prediction of the timing values for each of the bins satisfy the predetermined threshold.

80. The semiconductor device of claim 76, wherein the receiving the sign-off prototype further comprises receiving the sign-off prototype from a second party.

81. The semiconductor device of claim 80, wherein generating the second physical design of the circuit from the sign-off prototype further comprises having the third party to perform additional interactive optimization on the sign-off prototype after receiving the sign-off prototype so the second party can collaborate in resolving problems identified in the sign-off prototype.

82. A method for a first party to fabricate an integrated circuit comprising:

receiving a sign-off prototype, the sign-off prototype generated by:

performing estimates of physical area placement and timing analysis on a circuit design defined by a net list;

refining a physical placement of the circuit design based on the estimates of physical area placement and timing analysis; and

generating the sign-off prototype indicative of the refined physical placement of the circuit design; and

after receiving the sign-off prototype, the first party performing:

generating a second physical design of the circuit from the sign-off prototype;

generating a GDS file from the second physical design;

having a mask set generated from the GDS file; and

having the semiconductor device fabricated using the mask set.

83. The method of claim 82, wherein the refining the physical placement of the circuit design further comprises the repeatedly quantizing the circuit design into smaller and smaller bins and performing placement of cells and wires of the circuit design into the bins with each repetition.

84. The method of claim 83, further comprises for each repetition:

(a) creating a profile of the wire lengths versus the instances of nets for each of the bins;

(b) comparing the errors of prediction of timing values for each of the bins to the predetermined threshold;

repeating steps (a) and (b) until the all of the errors of prediction for each of the bins satisfy the predetermined threshold; and

generating the prototype based on the placement of the circuit design after all of the errors of prediction for each of the bins satisfy the predetermined threshold.

85. The method of claim 83, wherein the performing the second physical design of the circuit further comprises performing one or more of the following: placement of cells of the circuit design, logic optimization of the circuit design, routing of wires in the circuit design, timing and clock control for the circuit design and extraction of the circuit design.

86. The method of claim 82, wherein the sign-off prototype is received from a second party.

87. The method of claim 86, wherein generating the second physical design of the circuit from the sign-off prototype further comprises directing the second party to perform additional interactive optimization on the sign-off prototype after receiving the sign-off prototype so the second party can collaborate in resolving problems identified in the sign-off prototype.

88. A semiconductor device manufactured by:

receiving a sign-off prototype , the sign-off prototype generated by:

performing estimates of physical area placement and timing analysis on a circuit design defined by a net list;

refining a physical placement of the circuit design based on the estimates of physical area placement and timing analysis; and

generating the sign-off prototype indicative of the refined physical placement of the circuit design; and

after receiving the sign-off prototype, the first party performing:

generating a second physical design of the circuit from the sign-off prototype;

generating a GDS file from the second physical design;

having a mask set generated from the GDS file; and

having the semiconductor device fabricated using the mask set.

89. The semiconductor device of claim 88, wherein the refining the physical placement of the circuit design further comprises the repeatedly quantizing the circuit design into smaller and smaller bins and performing placement of cells and wires of the circuit design into the bins with each repetition.

90. The semiconductor device of claim 89, further comprises for each repetition:

(a) creating a profile of the wire lengths versus the instances of nets for each of the bins;

(b) comparing the errors of prediction of timing values for each of the bins to the predetermined threshold;

repeating steps (a) and (b) until the all of the errors of prediction for each of the bins satisfy the predetermined threshold; and

generating the prototype based on the placement of the circuit design after all of the errors of prediction for each of the bins satisfy the predetermined threshold.

91. The semiconductor device of claim 88, wherein the performing the second physical design of the circuit further comprises performing one or more of the following: placement of cells of the circuit design, logic optimization of the circuit design, routing of wires in the circuit design, timing and clock control for the circuit design and extraction of the circuit design.

92. The semiconductor device of claim 88, wherein the sign-off prototype is received from a second party.

93. The semiconductor device of claim 92, wherein generating the second physical design of the circuit from the sign-off prototype further comprises directing the second party to perform additional interactive optimization on the sign-off prototype after receiving the sign-off prototype so the second party can collaborate in resolving problems identified in the sign-off prototype.

94. A semiconductor device, comprising:

an integrated circuit segmented into a plurality of bins, the integrated circuit including;:

a first bin having a first group of nets optimized to a first set of criteria; and

a second bin having a second group of nets optimized to a second set of criteria,

wherein the first criteria and the second criteria are substantially different.

95. The semiconductor device of claim 94, wherein the first bin is designed to a first GDS level and the second bin is designed to a second GDS level.

96. A computer-readable medium including computer code configured to perform the design of an integrated circuit, the computer code including:

timing and placement tools that are configured to generate a prototype , the timing and placement tools including:

a resource and allocation and sharing module;

an implementation module;

a logic structuring module;

a technology mapping module;

a global optimization module; and

a prototype optimization tool; and

a prototype optimization tool that enables the optimization of the prototype.

97. The computer readable medium of claim 96, further comprising a reporting tool configured to generate a report on design features defined by the prototype.

98. The computer readable medium of claim 96, wherein the resource and allocation and sharing module; the implementation module; the logic structuring module; the technology mapping module; the global optimization module; and the prototype optimization tool operate sequentially.

99. The computer readable medium of claim 96, wherein the resource and allocation and sharing module; the implementation module; the logic structuring module; the technology mapping module; the global optimization module; and the prototype optimization tool operate in parallel.

100. The computer readable medium of claim 96, wherein the timing and placement tools further comprise a logic optimization tool, a routing tool, a timing and clock analysis tool, and an extraction tool.